features. Furthermore, a device or structure that is configured in a certain way is configured in at least that way, but may also be configured in ways that are not listed.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below, if any, are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of one or more aspects of the invention and the practical application, and to enable others of ordinary skill in the art to understand one or more aspects of the invention for various embodiments with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A structure comprising:

a semiconductor device comprising a substrate, the substrate comprising a p-type well adjoining an n-type well, and the semiconductor device comprising:

a first p-type region and a first n-type region disposed within the n-type well of the substrate, wherein the first p-type region at least partially encircles the first n-type region; and

a second p-type region and a second n-type region disposed within the p-type well of the substrate, wherein the second n-type region at least partially encircles the second p- type region,

wherein one of the p-type well or the n-type well of the substrate is located within the other of the p-type well or the n-type well of the substrate, and

wherein a portion of the n-type well of the substrate extends between first p-type region and the first n-type region, and a portion of the p-type well of the substrate extends between the second p-type region and the second n-type region.

2. The structure of claim **1**, wherein the first p-type region fully encircles the first n-type region within the n-type well and the second n-type region fully encircles the second p-type region within the p-type well.

3. The structure of claim **1**, wherein the semiconductor device comprises a bipolar junction transistor, the bipolar junction transistor comprising:

a base region and an emitter region, the base region comprising one of the first n-type region or the second p-type region and the emitter region comprising the other of the first n-type region or the second p-type region; and

a collector region and a ring region, the collector region comprising one of the first p-type region or the second n-type region and the ring region comprising the other of the first p-type region or the second n-type region.

4. The structure of claim **3**, further comprising:

an electrical contact structure, the electrical contact structure electrically connecting the ring region and the emitter region.

5. The structure of claim **3**, wherein the ring region encircles the emitter region.

6. The structure of claim **3**, wherein the ring region is configured to facilitate linearity of the bipolar junction transistor.

7. The structure of claim **1**, wherein the semiconductor device comprises a semiconductor controlled rectifier, the semiconductor controlled rectifier comprising:

a first section, the first section comprising the first p-type region;

a second section, the second section comprising the first n-type region;

a third section, the third section comprising the second n-type region; and

a fourth section, the fourth section comprising the second p-type region.

8. The structure of claim **1**, wherein the substrate comprises a first semiconductor material, and at least one region of the first p-type region, first n-type region, second p-type region, or second n-type region comprises a second semiconductor material, wherein the first and second semiconductor materials are different semiconductor materials.

9. The structure of claim **8**, wherein the first semiconductor material comprises silicon and the second semiconductor material comprises silicon germanium, and wherein the second semiconductor material of the at least one region is in at least partial crystal alignment with the first semiconductor material of the first substrate.

10. The structure of claim **1**, wherein the substrate comprises multiple fins, and at least one region of the first p-type region, first n-type region, second p-type region, or second n-type region comprises one or more fins of the multiple fins of the substrate.

11. The structure of claim **10**, further comprising at least one epitaxial contact structure, the at least one epitaxial contact structure contacting the one or more fins of the at least one region.

12. The structure of claim **1**, further comprising a p-type substrate contact region, wherein the p-type substrate contact region is spaced apart from both the p-type well and the n-type well, and electrically contacts the substrate.

13. A method comprising:

providing a semiconductor device comprising a substrate, the substrate comprising a p-type well adjoining an n-type well, and the providing comprising:

fabricating a first p-type region and a first n-type region disposed within the n-type well of the substrate, and a second p-type region and a second n-type region disposed within the p-type well of the substrate, wherein the first p-type region at least partially encircles the first n-type region, and the second n-type region at least partially encircles the second p-type region,

forming one well of the p-type well or the n-type well within the substrate; and

forming the other well of the p-type well or the n-type well within the one well,

wherein a portion of the n-type well of the substrate extends between first p-type region and the first n-type region, and a portion of the p-type well of the substrate extends between the second p-type region and the second n-type region.

14. The method of claim **13**, wherein the fabricating further comprises forming the first p-type region to fully encircle the first n-type region within the n-type well and the second n-type region to fully encircle the second p-type region within the p-type well.

15. The method of claim **13**, wherein the substrate comprises a first semiconductor material, and the fabricating comprises:

forming at least one region of the first p-type region, first n-type region, second p-type region, or second n-type